Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTIONS**

1. **V OUTPUT**
2. **V INPUT**
3. **GROUND**

**.019”**

**.037”**

**1 2**

**3**

**5U**

**MASK**

**REF**

**Top Material: Al**

**Backside Material: TiNiAg**

**Bond Pad Size: .004” X .004”**

**Backside Potential: GND**

**Mask Ref:**

**APPROVED BY: DK DIE SIZE .037” X .049” DATE: 1/24/23**

**MFG: ON SEMI /MOTOROLA THICKNESS .014” P/N: 79L05C**

**DG 10.1.2**

#### Rev B, 7/19/02